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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,646	08/22/2003	Guy Moshe Cohen	YOR920030328US1	8783

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EXAMINER	
PHAM, THANHHA S	
ART UNIT	**PAPER NUMBER**
2813	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/645,646	COHEN, GUY MOSHE	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12, 21-24, 28-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12, 21-24, 28-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 1/3/07, 7/25/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Amendment dated 10/11/2006.

Claim Objections

1. **Claim 12 is objected to because of informalities:**

line 1, "said device" should changed to --said double-gate field effect transistor--for clarifying the scope of the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1-12, 21-24, and 28-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Joshi (US006921982B2) previously applied.**

► With respect to claim 1, Joshi (fig. 8F, col. 10) discloses a double-gate field effect transistor (87) (see column 10 line 4) comprising:

a strained-silicon channel (16) formed adjacent a source (12) and drain (14) (see column 10 lines 9-10);

first gate (88) formed over a first side of said channel (16);

a second gate (89) formed over a second side of said channel (16);

a first gate dielectric (33) formed between said first gate and said strained-silicon channel (16) (see column 6 lines 13-18, gate on dielectric); and

a second gate dielectric (33) formed between said second gate and said strained-silicon channel (16) (see column 6 lines 13-18, gate on dielectric),

wherein said strained-silicon channel (16) is non-planar (figure 8F).

► With respect to claim 2, Joshi (fig. 8F) discloses that the strained-silicon channel (16) thickness is substantially uniform (figure 8F).

► With respect to claim 3, Joshi (fig. 8F, col. 10) discloses that the strained-silicon channel (16) thickness is set by epitaxial growth (column 8 lines 1-4).

► With respect to claim 4, Joshi discloses that the strained-silicon channel (16) is substantially defect-free (column 7 lines 18-20, high quality SiGe free from dislocations). It is noted that the strained-silicon channel (16) substantially defect-free considers as strained-silicon channel (SiGe) free from dislocations since the claimed "defect-free" is not defined the structure of the strained-silicon channel.

► With respect to claim 5, Joshi (fig. 8F, col. 10) discloses that the strained-silicon channel (16) includes a distorted lattice cell. This is inherent to a strained layer.

► With respect to claim 6, Joshi (fig. 8F, col. 10 line 11-14) discloses that the first gate (88) and the second gate (89) are independently controllable.

► With respect to claim 7, Joshi (fig. 8F, col. 10 line 4) discloses that the strained silicon channel (16) comprises a fin.

► With respect to claim 8, Joshi (fig. 8F) discloses that the first and second gates are self-aligned.

► With respect to claim 9, the limitation of forming the first and second gates in a single lithography step is a process limitation (product by process) and has no patentable weight in device claims. Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production." MPEP 2113

► With respect to claim 10, Joshi (fig. 8F) discloses that the first gate and second gate, the source and the drain are self-aligned with respect to each other.

► With respect to claim 11, the background of the invention teaches that it is known to use one or more fins (column 1 line 42-44). Also see column 7 lines 64-65 and column 8 lines 42-43).

► With respect to claim 12, Joshi (fig. 8F) discloses that the double-gate field effect transistor includes a planarized top surface.

► With respect to claim 28, Joshi (fig. 8F) discloses that the first gate (88) is separated from the second gate (89).

► With respect to claim 32, the claim is a product by process claim and the process is given no patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product

itself. The patentability of a product does not depend on its method of production." MPEP 2113

► With respect to claim 34, Joshi (fig. 8F, column 10 line) discloses that the strained-silicon channel is controlled by said first gate (88) and by the second gate (89). Furthermore, "When the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent" MPEP 2112.01 1. As the structure of claim 1 is that taught by Joshi, it is inherent the same function is inherent.

► With respect to claim 36, Joshi (fig. 8F) discloses that the first gate (88) and the second gate (89) are separated from one another.

► With respect to claim 37, Joshi (fig. 8F, column 10) discloses that carriers in the channel are inherently controlled by the first gate and the second gate. Furthermore, "When the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent" MPEP 2112.01 1. As the structure of claim 1 is that taught by Joshi, it is inherent the same function is inherent.

► With respect to claim 38, Joshi (fig. 8F) discloses that the channel (16) a first vertical surface covered by the first gate dielectric (33) and a second vertical surface covered the second gate dielectric (33).

► With respect to claim 21, Joshi (fig. 8F, col. 10) discloses a double-gate field effect transistor (87) (see column 10 line 4) comprising:

a strained-silicon channel (16) formed adjacent a source (12) and drain (14) (see column 10 lines 9-10);

first gate (88) formed over a first side of said channel (16);

a second gate (89) formed over a second side of said channel (16);

a first gate dielectric (33) formed between said first gate and said strained-silicon channel (16) (see column 6 lines 13-18, gate on dielectric); and

a second gate dielectric (33) formed between said second gate and said strained-silicon channel (16) (see column 6 lines 13-18, gate on dielectric),

wherein said strained-silicon channel (16) comprises a fin (column 10 line 4).

► With respect to claim 22, Joshi (fig. 8F, col. 10) discloses that a circuit may comprise the double-gate field effect transistor of claim 1 (column 1 lines 14-45).

► With respect to claim 23, Joshi (fig. 8F, column 5 lines 40-45) discloses that the strained silicon channel (16) is tensely strained.

► With respect to claim 24, Joshi (fig. 8F, column 5 lines 40-45) discloses that the strained silicon channel (16) is compressively strained.

► With respect to claim 29, Joshi (fig. 8F) discloses that the first gate (88) is separated from the second gate (89).

► With respect to claim 33, the claim is a product by process claim and the process is given no patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production." MPEP 2113

► With respect to claim 35, Joshi (fig. 8F, column 10 line) discloses that the strained-silicon channel is controlled by said first gate (88) and by the second gate (89). Furthermore, "When the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent" MPEP 2112.01 1. As the structure of claim 1 is that taught by Joshi, it is inherent the same function is inherent.

► With respect to claim 30, Joshi (fig. 8F, col. 10) discloses a double-gate field effect transistor (87) (see column 10 line 4) comprising:

a strained-silicon channel (16) formed adjacent a source (12) and drain (14) (see column 10 lines 9-10);

first gate (88) formed over a first side of said channel (16);

a second gate (89) formed over a second side of said channel (16);

a first gate dielectric (33) formed between said first gate and said strained-silicon channel (16) (see column 6 lines 13-18, gate on dielectric); and

a second gate dielectric (33) formed between said second gate and said strained-silicon channel (16) (see column 6 lines 13-18, gate on dielectric),

wherein said strained-silicon channel (16) is non-planar, and the first and second sidewalls are opposing to each other (figure 8F).

► With respect to claim 31, Joshi (fig. 8F, col. 10) discloses a double-gate field effect transistor (87) (see column 10 line 4) comprising:

a strained-silicon channel (16) formed adjacent a source (12) and drain (14) (see column 10 lines 9-10);

first gate (88) formed over a first side of said channel (16);

a second gate (89) formed over a second side of said channel (16);

a first gate dielectric (33) formed between said first gate and said strained-silicon channel (16) (see column 6 lines 13-18, gate on dielectric); and

a second gate dielectric (33) formed between said second gate and said strained-silicon channel (16) (see column 6 lines 13-18, gate on dielectric),

wherein said strained-silicon channel (16) is non-planar, and is fixed to a substrate (20) by the first and second gates.

It is noted that the claim limitation "elastically induced by a sacrificial stressor" is a product by process claim and the process is given no patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production." MPEP 2113

Response to Arguments

3. Applicant's arguments filed 10/11/2006 have been fully considered but they are not persuasive.

Applicant argues that Joshi does not teach or suggest "a double-gate field effect transistor", as recited in claim 1, and similarly recited in claims 21, 30 and 31.

Applicant's argument is not persuasive because Joshi clearly disclose a double-gate field effect transistor (87) having the first gate (88) and the second gate (89) (see

fig. 8F, column 10 lines 4-5). Therefore, Joshi meets and anticipates the claimed invention.

Applicant argues that "*the channel 8 (Si Fin) has two vertical surfaces. Each of these surfaces is covered with a gate oxide and is gated by gate 1 and gate 2, respectively. The carriers in the channel are therefore controlled effectively by gate 1 and gate 2. This is not the case for the carriers in channel 32 of Joshi, where the two gates are distanced by the core 24. Even if core 24 were made ultra thin, there is no gate oxide that coats the inner surface of channel 32. As a result, only one surface of the channel 32 is gated as the other (inner) surface is in contact with the core 24 and is not gated*".

Applicant's argument is not persuasive because there is no basic for this statement "*the channel 8 (Si Fin) has two vertical surfaces. Each of these surfaces is covered with a gate oxide and is gated by gate 1 and gate 2, respectively*". Moreover, Joshi (fig. 8F) clearly discloses the channel (16) has two vertical surfaces. Each of these surfaces is covered with a gate oxide (33) and is gated by gate (88) and gate (89), respectively. It is noted that, the core (24) is part of the channel (16)(see column 5 lines 10-33).

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

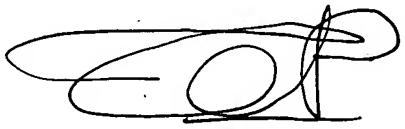
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



TSP

THANHHA S. PHAM
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